LISTING OF THE CLAIMS:

Claim 1. (original) A method for forming a low resistance MOSFET device comprising the steps of:

forming a gate region atop a surface of substrate;

forming first spacers having a first spacer width on sidewalls of said gate region;

forming first silicide regions having a first silicide thickness in said substrate as well as atop a surface of said gate region;

forming second spacers having a second width greater than said first spacer width on said substrate, wherein said second spacers protect said first silicide region in said substrate; and

forming second silicide regions in said substrate and atop a surface of said gate region, wherein said second silicide regions have a thickness that is greater than said first silicide thickness

Claim 2. (original) The method of Claim 1 wherein said forming of said gate region further comprises predoping of said gate region.

Claim 3. (original) The method of Claim 2 wherein said predoping is performed by ion implantation of a type III-A element or a type V element into said gate region.

Claim 4. (original) The method of Claim 3 where predoping is achieved via ion implantation of phosphorus into said gate region.

Claim 5. (original) The method of Claim 1 further comprising the step of forming source/drain extension regions following said gate region formation.

Claim 6. (original) The method of Claim 1 wherein said first spacer width is from about 5nm to about 20 nm.

Claim 7. (original) The method of Claim 1 wherein said first spacer width is from about 7 nm to abut 15 nm.

Claim 8. (original) The method of Claim 1 wherein said second spacers width is from about 20 nm to about 90 nm.

Claim 9. (original) The method of Claim 1 wherein said second spacers width is from about 30 nm to about 70 nm.

Claim 10. (original) The method of Claim 1 further comprising the steps of forming deep source/drain regions after forming said first spacers.

Claim 11. (original) The method of Claim 10 wherein forming said deep source/drain regions comprises ion implantation of a type III-A element or a type V element into said substrate.

Claim 12. (original) The method of Claim 1 wherein said forming of said first silicide region comprises depositing a first metal layer upon an exposed surface of said substrate and annealing.

Claim 13. (original) The method of Claim 12 where said first metal layer has a thickness from about 2 nm to about 7 nm.

Claim 14. (original) The method of Claim 13 where said first metal layer comprises Ta, Ti, W, Pt, Co, Ni, or combinations thereof.

Claim 15. (original) The method of Claim 1 wherein said first silicide regions have a thickness of about 1nm to about 20 nm.

Claim 16. (original) The method of Claim 1 wherein said first silicide regions have a thickness from about 2 nm to about 15 nm.

Claim 17. (original) The method of Claim 1 wherein said first silicide regions have a thickness from about 5 nm to about 12 nm.

Claim 18 (original) The method of Claim 1 wherein said first silicide region is formed in said substrate having a channel region beneath said gate region, where the distance between said silicide region and said channel region is from about 2 nm to about 15 nm.

Claim 19. (original) The method of Claim 1 wherein said first silicide region is formed in said substrate having a channel region beneath said gate region, where the distance between said silicide region and said channel region is from about 3 nm to about 10 nm

Claims 20-33 (canceled)